

# Structural design points in arrayed micro thermal sensors (II) ~ Experimental verification ~

Hirofumi Miki, S. Tsuchdani

**Abstract—** Previously, we reported the structural design points in arrayed micro thermal sensors by utilizing electrical-thermal analogies and simulation analysis. In this paper, the applicable structure of arrayed micro thermal sensor are discussed based on our previous results of simulation analysis, and demonstrated the effectiveness of the design points experimentally using fabricated prototype that based on silicon approach.

**Index Terms—** MEMS, thermal sensor, array sensor, fingerprint capture, structural design.

## I. INTRODUCTION

In the application to measure physical information like temperature or flow micro thermal sensors have been widely used, and it is also possible even in the application of fingerprint pattern capture. Generally, silicon micro machining was used in the fabrication of these sensors, due to the possibility of integration with IC on the same sensor chip, and its well-established technology. However, particular attention is necessary because silicon possesses features of high thermal conductivity and mechanical brittleness. In micro thermal sensor design, the most important aspects are sensitivity, response speed, and mechanical strength. As far as the sensitivity is concerned, the contribution of the sensing-information independent heat transfer (e.g., flow-independent heat transfer in flow sensor) should preferably be small. To achieve this, the sensing area must be thermally isolated from its supporting structure sufficiently. The simplest structure can be formed by a closed membrane. In a square area in the center of the chip the major part of the silicon is etched away from the back of the chip, leaving only a thin diaphragm at the surface with a thickness of typically a few microns. By etching away parts of the membrane surface as well, cantilever beams, bridges and suspended membranes can be formed. To realize an array layout of these single elements, there are new thermal design issues compared to those of the single thermal sensors. Bulk and surface micromachining technology has been employed to realize array type thermal sensors<sup>[1-3, 5-13]</sup>.

In bulk micromachining by anisotropic wet etching, the design freedom is limited by the crystallographic structure of the wafer, results in the limitations of the miniaturization in arrayed element size. When fabricate a thermal isolation diaphragm structure on a (100) silicon wafer (thickness: d) by

backside anisotropic wet etching, there exists a length limit of  $l_{min} = 2d(\cot 54.74^\circ)$  due to the inclined walls given by the etch-stopping planes (111 of crystal orientation). The size of the array cell should not be shorter than the length in the corresponding direction. By front-side undercut etching, denser of the elements array is possible<sup>[13]</sup>.

Surface micromachining enables small structures and offers a high freedom of design, however, the maximum gap distance between the functional layers and the silicon substrate is typically only several  $\mu\text{m}$ <sup>[4]</sup>. Drawbacks of surface micromachining are stress in the structure film, and possible sticking of the structures to the substrate<sup>[4]</sup>. These problems are especially critical in the application of tactile sensors like the fingerprint captures. Comparing to the surface micromachining, bulk micromachining technology is a well-established and understood technology, provides a reliable industrial process and requires only a small investment for the etching equipment. Further, by bulk micromachining, the problem of sticking between the diaphragm and the substrate can be avoided.

To examine and verify an optimum structural design points in thermal sensors, we developed micro fabrication process for the thermal sensor prototype and fabricated silicon and polymer based prototype of arrayed micro sensor device by utilizing bulk micromachining and polymer wet-etching technology. In this paper, the evaluation results in the sensor properties based on silicon-based approach are reported.

## II. STRUCTURAL DESIGN AND FABRICATION

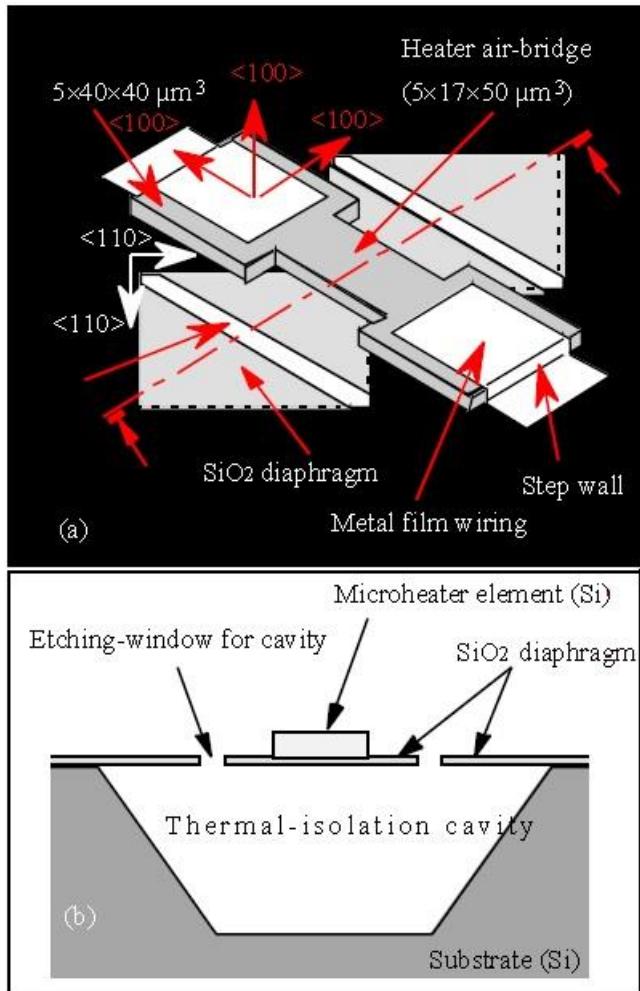
*(Silicon-based approach)*

### A. Basic prototype

Before the real fabrication process, we confirmed and analyzed the structure formation utilizing MICROCAD simulation. The software MICROCAD is a three-dimensional (3-D) wet etching simulator co-developed by Fuji Research Institute Co. (now Mizuho Information & Research Institute), and Nagoya University<sup>[14]</sup>. It is equipped with a database of orientation-dependent etching rates for the single crystal silicon. The basic structure for the proposed sensor device is shown in Fig. 1.

**Hirofumi Miki**, Dept. of Systems Engineering Wakayama University 930, Sakaedani, Wakayama, Japan

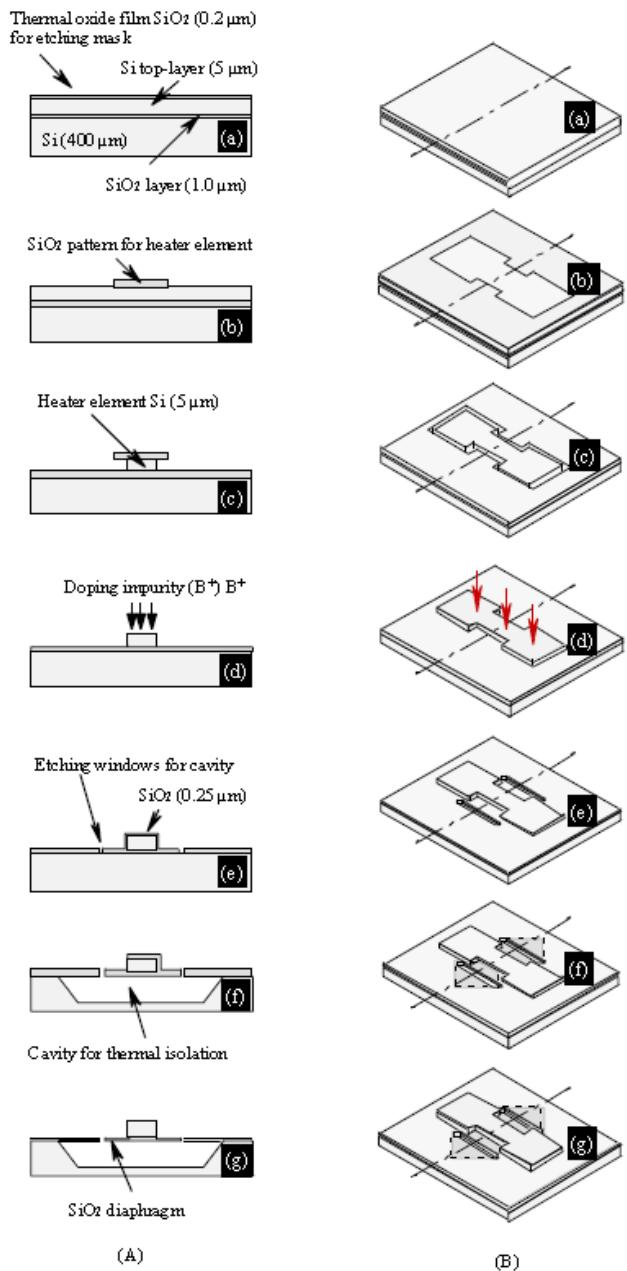
**S. Tsuchdani** Dept. of Systems Engineering Wakayama University 930, Sakaedani, Wakayama, Japan



**Fig. 1** Structure of the proposed thermal type micro fingerprint capture (a: top view, b: cross-sectional view). This model was utilized in the simulation calculation and experimental evaluations.

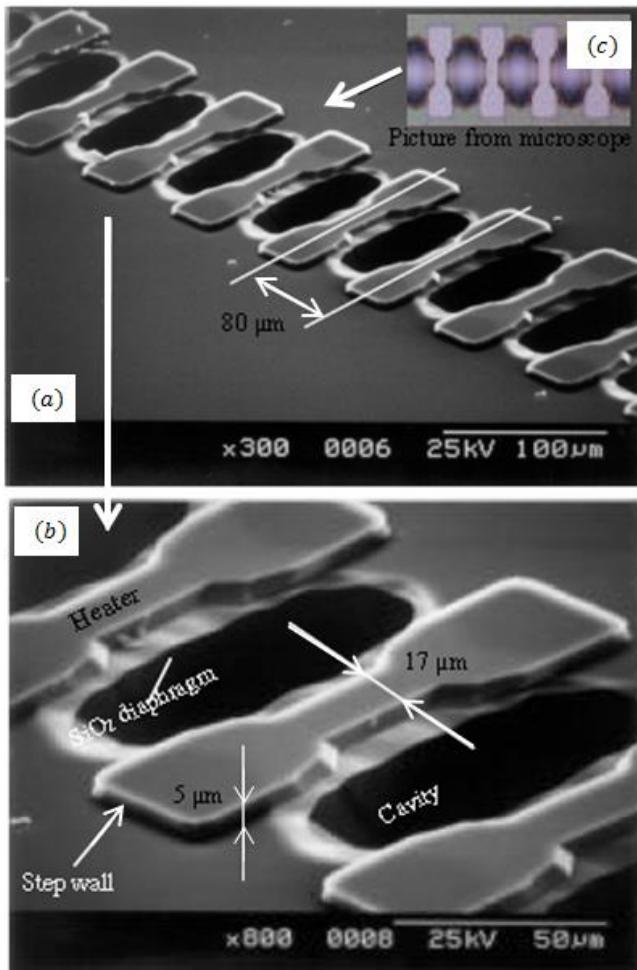
In device fabrication, a p-type (100) SOI (*Silicon on Insulator*) wafer was used as the starting material. It had a 400- $\mu\text{m}$ -thick substrate and 5- $\mu\text{m}$ -thick top layer sandwiching a 1- $\mu\text{m}$ -thick  $\text{SiO}_2$  insulation layer. The direction of the orientation flat was  $<100>$ , both in the substrate and in the top layer, and the resistivity of the top layer silicon was 5- $\Omega\text{ cm}$ . Figure 2 shows the simplified fabrication process flow.

The Fabrication process starts with the formation of thermal dioxide layer (0.2- $\mu\text{m}$   $\text{SiO}_2$ ) at 1000 (step a). By etching the  $\text{SiO}_2$  layer in BHF (50% HF: 40%  $\text{NH}_3\text{F}$ = 1:6) solution, etching mask patterns for the heater element were formed (step b). By etching the top layer silicon in TMAH (25wt%, 80°C), 5- $\mu\text{m}$  thick heater elements were formed (step c).  $5 \times 10^{15}$  (atoms/ $\text{cm}^2$ ) of boron impurity was doped to the heater elements to decrease the resistivity to the value of 0.02- $\Omega\text{ cm}$  (step d). To create the thermal isolation cavity and diaphragm structure under the heater elements, etching window patterns were formed on the  $\text{SiO}_2$  layer after thermally oxidizing again to form the protective coating on the heater elements (step e). By front-side undercut etching in TMAH (25wt%, 80°C) solution, the designed cavity and diaphragm structure was realized (step f). For electrical contact, the protective coating of  $\text{SiO}_2$  layer on the heater elements was etched out (step g).

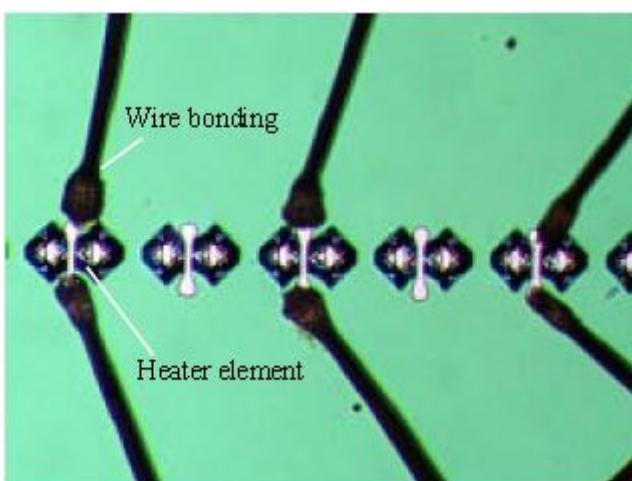


**Fig. 2** Fabrication process flow for the proposed prototype: (A) Cross-sectional views, and (B) 3D views of the device structure.

Figure 3 shows a SEM picture of the fabricated first prototype. Fig. 3-(a) presents the arrayed micro heater elements whose structure contains a diaphragm and a laterally interpenetrated cavity under each element, and (b) is the enlarged view of the (a), and (c) is an optical microscopy image of the (a). At this stage, it is found that the deposition of a thin metal film for wiring become in an open circuit on the step-wall of the 5- $\mu\text{m}$  height heater pad due to the poor coverage of the metal. In wire bonding, 25~50- $\mu\text{m}$  diameter aluminum or gold wires are used generally. It is also found that a direct bonding to the pad is not an appropriate way due to the large thermal capacity of the wire and the possibility of a big amount of the heat loss through it. Figure 4 shows an optical microscopy picture after wire bonding was performed directly on the pad using 30- $\mu\text{m}$  diameter aluminum wires.

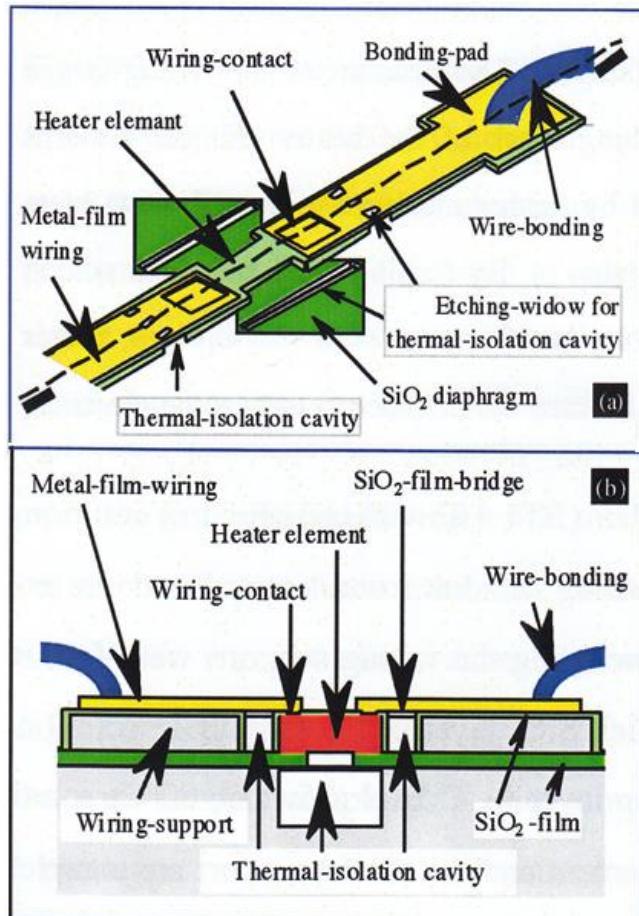


**Fig. 3** SEM picture of the first prototype: (a) Arrayed micro heater elements consisting of a diaphragm and a laterally interpenetrated cavity under each element; (b) Enlarged view of (a), and (c) Optical microscopy image of (a).



**Fig. 4** Optical microscopy picture after wire bonding (Wiring:  $\phi 30\text{-}\mu\text{m}$  of aluminum wire).

It is possible that a great amount of heat loss might be generated due to the large thermal capacity of the wiring and the path of the heat flow through wire. To avoid these problems, we improved the structure as shown in Fig. 5.



**Fig. 5** Improved structure to avoid open circuit in wiring and decrease the heat loss via wiring: (a) 3D view, and (b) cross-sectional view of the proposed structure.

#### B. Improved prototype

In the improved version, a wiring-support structure was proposed. Each heater element was separated from the wiring-support by a thermal isolation cavity in the length direction. Over this cavity, 1.5- $\mu\text{m}$  thick  $\text{SiO}_2$ -film-bridges were arranged for the thin metal film wiring. The heater element and wiring-support surfaces were thermally oxidized for electrical and thermal insulation. Then a thin metal film was coated on from the heater element to the bonding pad, which is apart from the heater element, across the  $\text{SiO}_2$ -film-bridges. In this way, the problem of open circuit on the heater step-wall can be avoided during metal film deposition. In addition, the problems of large heat capacity in the heater element and the large amount of heat loss via wiring will be reduced too.

The fabrication process flow for the improved structure is shown in Fig. 6. Figure 6-A shows the 3D views and Fig. 6-B the cross-sectional views of the structure. The starting material is the same as that of the basic prototype. Firstly, to fabricate the heater and wiring-bridge patterns, the wafer surface was thermally oxidized to a thickness of 1.5- $\mu\text{m}$  at 1000°C (step a). The patterns for the wiring-bridge and the etching windows were formed by etching the  $\text{SiO}_2$  layer to the thickness of 0.3- $\mu\text{m}$  in BHF (50% HF: 40%  $\text{NH}_3\text{F}$  = 1:6) solution (step b).

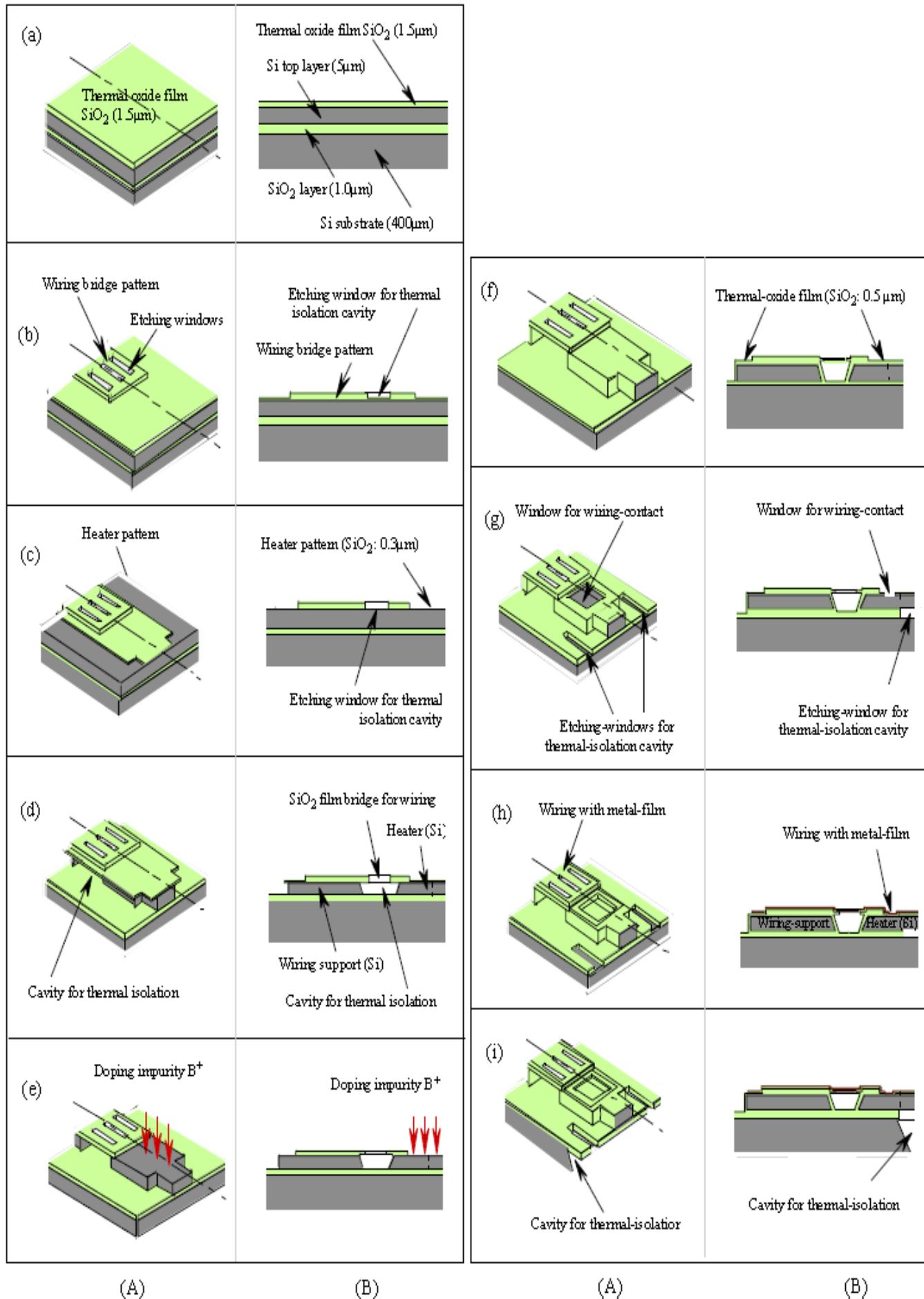
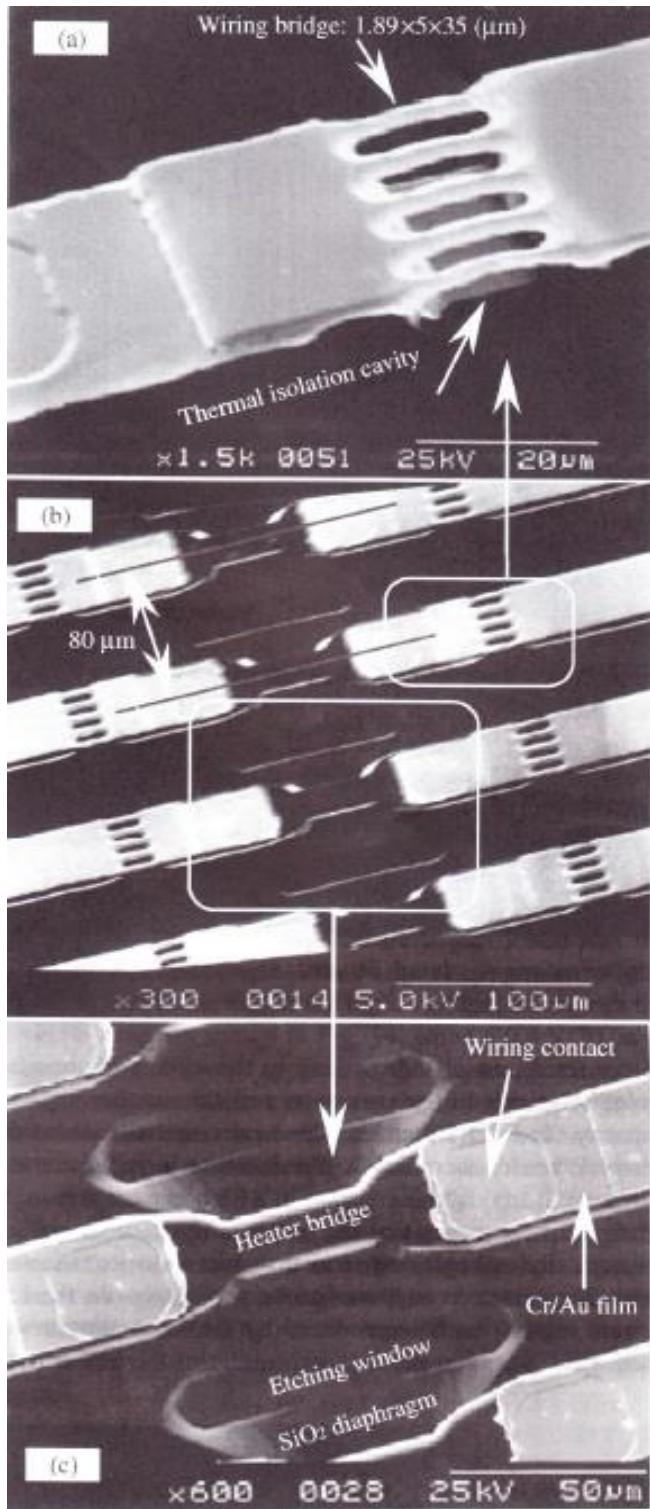


Fig. 6 Fabrication process flow of improved structure for the metal-film wiring: (A) 3D views, and (B) cross-sectional views.



**Fig. 7** SEM pictures of the improved prototype having Au/Cr (0.37- $\mu$ m/0.02- $\mu$ m) thin metal-film wiring: (a) Enlarged view of the wiring-bridge structure after thin metal-film coating, (b) Completed micro heater element array having laterally interpenetrated thermal isolation cavities and thin metal-film wiring across the wiring-bridge, (c) Enlarged view of the heater element structure.

The structure of the wiring-bridge etching windows was created and the etching mask of the heater element patterns (including the wiring support) were formed by further etching the rest of the 0.3- $\mu$ m thick SiO<sub>2</sub> layer in the same BHF solution (step c). By etching the 5- $\mu$ m thick silicon top layer in TMAH (25wt.%, 80°C) solution, the structures of wiring-bridges, heater element and the wiring support are

completed (step d). In order to reduce the electrical resistivity of the heater element, boron impurities were doped. Before doping, the SiO<sub>2</sub> layer on the heater surface must be removed. By doping  $5 \times 10^{15}$  atoms/cm<sup>2</sup> of boron, the electrical resistivity of the heater element was reduced from the original 5- $\Omega$  cm to 0.02- $\Omega$  cm (step e). By additional thermal oxidation again at 1000°C, a 0.5- $\mu$ m thick SiO<sub>2</sub> layer for electrical insulation was formed on the surfaces of the heater element and wiring-support (step f). By SiO<sub>2</sub> etching again in BHF, the wiring-contact windows on the heater surface and the etching window patterns for the thermal isolation cavity under the heater element were opened (step g). By sputtering 0.37- $\mu$ m thick Au using 0.02- $\mu$ m thick Cr layer as the adhesion promoter, the thin metal-film wiring was realized following with the lift-off patterning (step h). Finally, the laterally interpenetrated thermal-isolation cavity under each heater element was realized by etching the silicon in TMAH (25wt.%, 80°C) solution (step i).

Figure 7 shows the SEM pictures of the newly fabricated improved structure having thin metal-film wiring. Figure 7-(a) shows the enlarged view of the wiring-bridge with the size of 1.89  $\times$  5  $\times$  35 ( $\mu$ m<sup>3</sup>), having thin Au/Cr (0.37- $\mu$ m/0.02- $\mu$ m) coating. Figure 7-(b) shows the fabricated micro heater element array having the heater size of 5  $\times$  17  $\times$  50 ( $\mu$ m<sup>3</sup>) and a pitch of 80- $\mu$ m with a laterally interpenetrated thermal isolation cavity under the heater element. Thin metal-film wiring was coated across the wiring-bridge from the heater element to the wire-bonding pad. Figure 7-(c) is the enlarged view of the heater element structure. By means of the wiring-support structure, the open circuit problem is solved. By using thin metal-film wiring, the thermal capacity of the wiring and the heat-loss via the bonding wires will be greatly reduced.

After wire bonding, annealing was performed under 300°C for 30min to reduce the contacting resistance and simple packaging was performed for the experiments. The fabricated prototype was utilized in the experiments to evaluate its electrical and thermal properties.

### III. EXPERIMENTAL RESULTS AND EVALUATION

In order to evaluate the properties of the sensor, three important characteristics were measured: temperature coefficient of resistance (TCR), sensitivity and response time.

#### A. TCR of the heater element

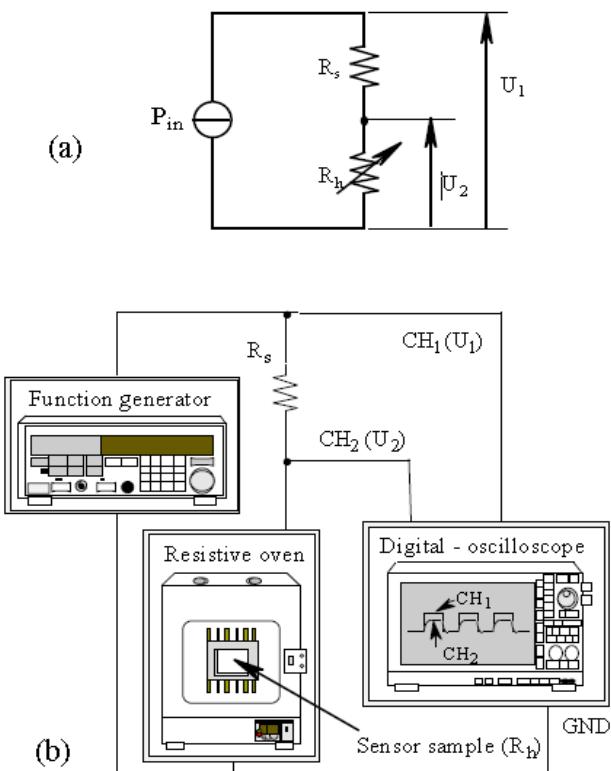
In the thermal sensor, sensing is realized due to the nonzero TCR of the heater element. TCR was obtained by measuring its resistance-change along with the temperature. The ambient temperature was well controlled using a precise resistive oven, inside of which the sample prototype was arranged. In these experiments, the temperature of the oven was increased by steps of 10°C from room temperature to 180°C. At every step, the temperature was stabilized for 30minutes and then the measurement was initiated.

Figure 8 shows the schematic illustration of the detection circuit and the experimental set-up. In Fig.8-a,  $R_s$  is the standard electrical resistance, and  $R_h$  is the temperature dependent electrical resistance of the micro heater element. The circuit was driven by a pulse voltage (or a constant

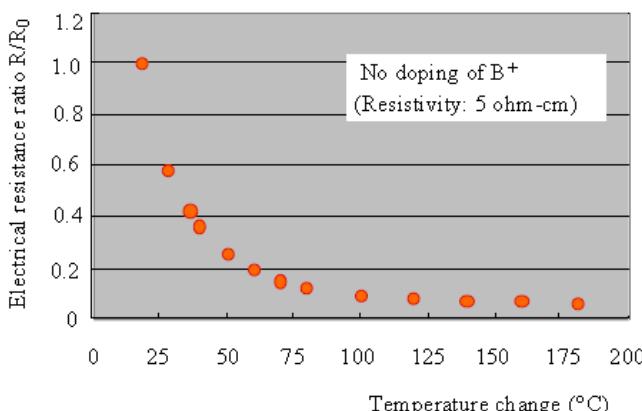
current) using the least input power to avoid the self-heating as much as possible. Using the following equation (1), the temperature dependent parameter  $R_h$  is easily measured in terms of known reference resistors  $R_s$  by the voltage drops across them.

$$R_h = \left( \frac{U_2}{U_1 - U_2} \right) R_s \quad (1)$$

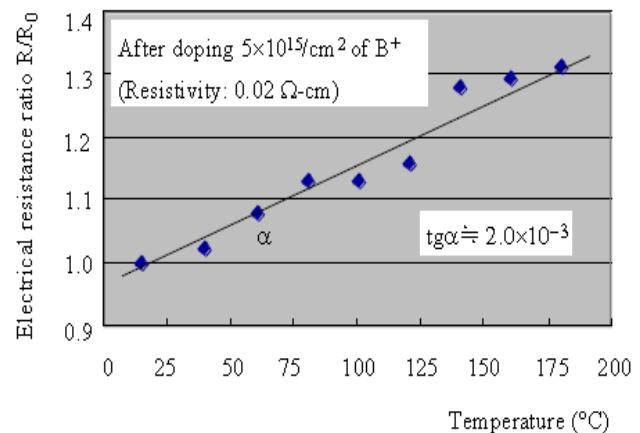
Where,  $U_1$  is the driving voltage across the reference resistance  $R_s$  and heater element  $R_h$ , and  $U_2$  is the voltage drop across the heater element  $R_h$ . Figures 9 and 10 show the temperature dependence of the heater element's resistance measured by the circuit of Fig.8 and calculated by equation (1).



**Fig. 8** Experimental set-up: (a) Detection circuit, and (b) Schematic illustration of the experimental set-up.  $R_s$  is the standard electrical resistance, and  $R_h$  is the temperature dependent electrical resistance of micro heater element.



**Fig. 9** Electrical resistance ratio of heater element versus temperature rise (no doping).



**Fig. 10** Electrical resistance ratio of heater element versus the temperature rise after B+ was doped.

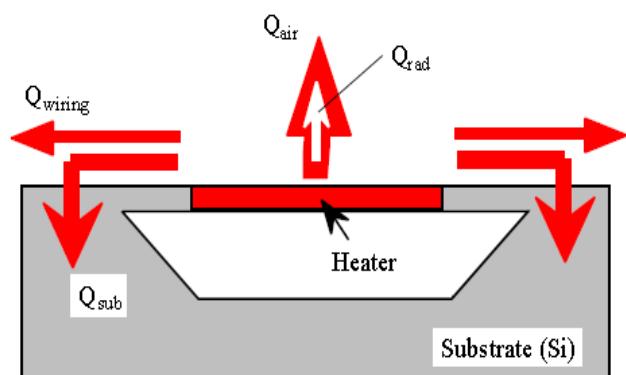
In Fig. 9, where no impurity was doped to the heater element, the electrical resistivity is 5- $\Omega$  cm. At the lower temperature range, the heater element showed a large negative TCR and very nonlinear resistance change along with the temperature. During the temperature rise from room temperature to the near 100 °C, the TCR changes largely.

In 18-50 °C, the TCR change was  $-23.3 \times 10^{-3} \text{K}^{-1}$ , and in 18-100 °C it was  $-10.98 \times 10^{-3} \text{K}^{-1}$ . The nonlinear resistance change with temperature (varying TCR) is only a slight disadvantage, because it is possible to make linearized analogue circuits or digital calibration routines at low cost<sup>[15]</sup>.

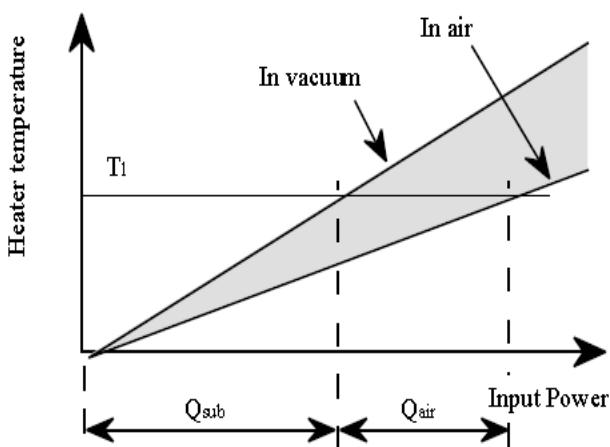
In Fig.10, where  $5 \times 10^{15}$  atoms/cm<sup>2</sup> of boron was doped to the heater element, the electrical resistivity was reduced to the value of 0.02- $\Omega$  cm. During the temperature rise of 14-180 °C, the heater element showed a positive TCR of about  $2.0 \times 10^{-3} \text{K}^{-1}$  with a good linearity. By adjusting the dopant concentration, the resistivity of silicon and its TCR could be easily controlled<sup>[16-19]</sup>. As a thermal-type fingerprint sensor, it is favorable to possess a higher value of TCR for the sensitivity. The following experiments were performed by using the sample that has no doping with impurity.

#### B. Thermal properties (Analysis of heat transfer)

Figure 11 schematically shows the path of the heat loss from the heater element. Where,  $Q_{air}$  and  $Q_{rad}$  respectively show the heat loss to the air by convection and radiation, while  $Q_{sub}$  and  $Q_{wiring}$  respectively show that of the substrate and wiring by conduction.



**Fig. 11** The path of consumed heat flow from the heater element.



**Fig. 12** Heat generated in the heater can be separated to be: (1) to the substrate of the device  $Q_{sub}$ , and (2) to the air in the ambient  $Q_{air}$ .

In the fingerprint sensor application, heater temperature will not be so high, that the heat loss by radiation  $Q_{rad}$  is small enough to be ignored. To understand the heat loss of  $Q_{air}$  and  $Q_{sub}$  separately is useful for the structural design in order to effectively control the heat transfer. For simplifying, from the following descriptions the heat loss through wiring  $Q_{wiring}$  is considered involved in  $Q_{sub}$ . In vacuum, the heat generated in the heater will be transferred to the substrate (including wiring) only, while in air it will be transferred to both the substrate and air at the same time. As shown in Fig. 12, by comparing the curves of temperature versus input power between in vacuum and in air, one can separate the heat loss to the air and the substrate. Where, the curve of temperature versus input power was got from the current-voltage curve and TCR of the heater. In order to get  $T_1$  of the temperature on the heater element, in air will need  $Q_{air}$  more of the input power than in vacuum. To reach  $T_1$  on the heater element, at least  $Q_{sub}$  of the input power is necessary. The better is the thermal isolation (between the heater and the substrate), the little the required input power. In thermal sensor, such a structure that shows smaller of  $Q_{sub}$  and larger of  $Q_{air}$ , at the same input power will result in better of sensitivity.

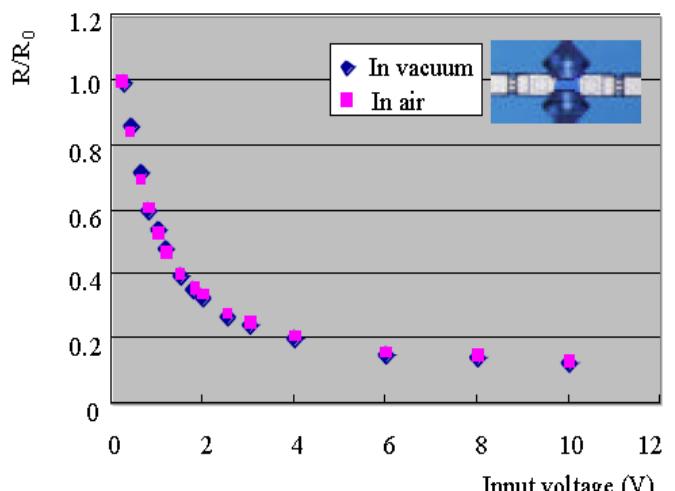
#### C. Effect of thermal isolation cavity

Experiment was performed respectively in air and in vacuum, to evaluate thermal isolation on the designed structure. Figure 13 shows the relationship of the heater resistance ratio versus input power. Due to the great temperature dependence of the heater resistance and the small thermal capacity of the heater element, the resistance ratio change along with the input power is tremendous, which can be applicable for the application of high sensitive micro temperature sensor or flow sensors. However, there are only slight differences in heater resistance ratio between in vacuum and in air ambient. It means that the heat from the heater dominantly transferred to the substrate. In order to increase the thermal isolation, the cavity was enlarged from the original depth of 40- $\mu$ m to the near 100- $\mu$ m by XeF<sub>2</sub> isotropic dry etching. This enlarged cavity makes the supporting pad of the heater element reaches near the boundary of the limit as shown in Fig. 14. Thermal isolation by enlarged cavity was evaluated using the same method as in Fig. 13. The

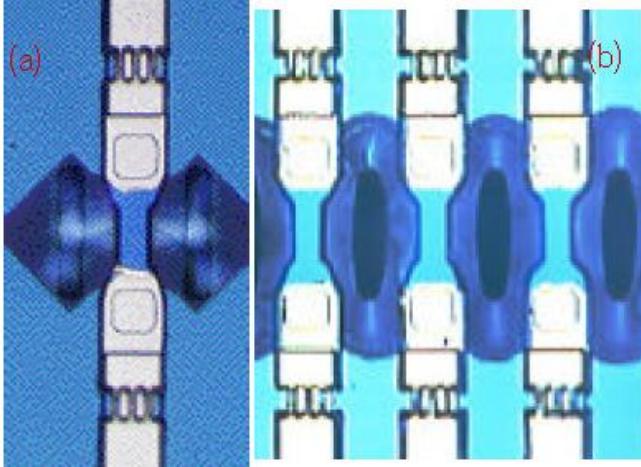
experimental results show that there is only a slight change after the cavity was enlarged (Fig. 15). In order to realize applicable sensor sensitivity, the cavity needs to be enlarged further by etching out the substrate even to the whole area of sensing element including the wiring-contact. By this solution, the applications of distribution measurement like temperature or flow become much advantageous, but for the application of fingerprint sensor, it is a desirable way to fill the etched cavity with insulation materials to ensure enough strength for the fingertip pressure.

#### D. Effect of wiring-bridge structure

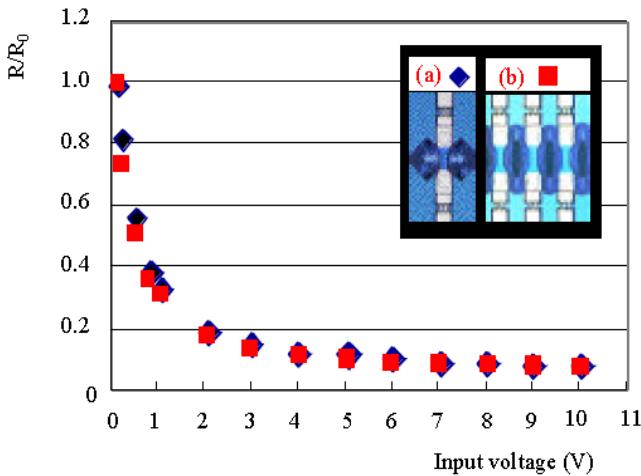
In thermal sensor, the heat loss through wiring is not ignorable and must be well controlled. To investigate the structural effect of the wiring-bridge to the thermal isolation and sensor properties, the following three prototypes having different structures are fabricated and experiment was performed to measure the heater resistance-ratio-change versus input power. Prototypes are as below: a) No thermal isolation cavity and no wiring-bridge, (b) No thermal isolation cavity, but having the wiring-bridge, and (c) Having both the thermal isolation cavity, and the wiring-bridge. Experimental results show that the structure of the wiring-bridge is effective for the thermal isolation as shown in Fig. 16. Comparing to the structure of (a), structure (b) and (c) showed larger of decrease in the heater resistance change, owing to the effects of wiring-bridge structure and the smaller thermal capacity. Near the input current 0.3mA, the heater temperature change became slowdown, and near the 1mA, the heater temperature trends to a constant. According to the TCR, it was understood that at 1mA, the heater temperature reached about 70 °C in the sensor structure (b) and (c), and 50 °C in that of (a). By means of wiring-bridge structure, about 20 °C more of temperature rise was realized. As for the structure that with and without cavity under the heater element, only a slight difference is confirmed as the thermal isolation effect (see Fig. 16-b & c). The reason supposed to be as below: (i) Both ends of the heater element were located on the substrate, so the heat could be transferred from the heater ends to the silicon substrate overwhelmingly; (ii) 1- $\mu$ m of SiO<sub>2</sub> layer cannot efficiently shut off the flow path from the heater element to the substrate.



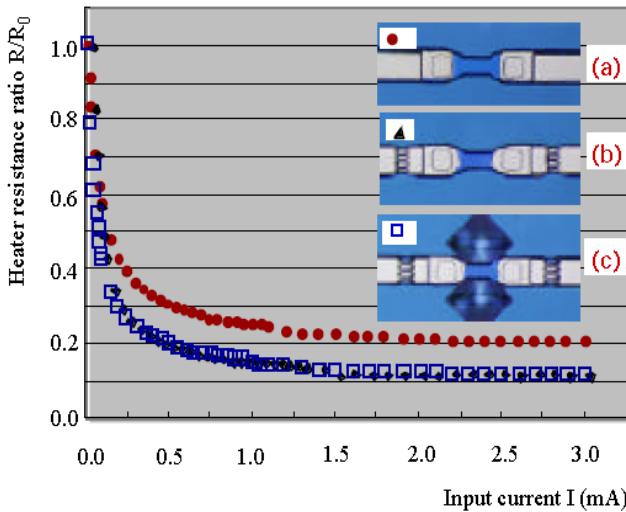
**Fig. 13** Thermal isolation effects of the cavity full of air and vacuum (Cavity is fabricated underneath the heater element).



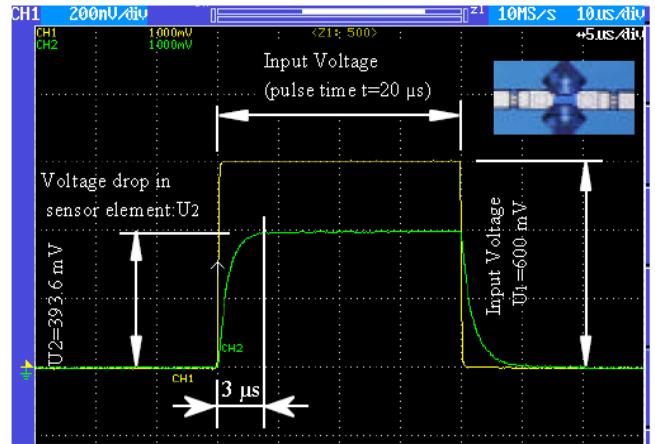
**Fig. 14** Enlarged cavity by  $\text{XeF}_2$  isotropic dry etching ( $2\text{XeF}_2 + \text{Si} \rightleftharpoons 2\text{Xe} + \text{SiF}_4$ ): (a) Before dry etching, and (b) After dry etching for the cavity enlargement.



**Fig. 15** Evaluation of thermal isolation effect by enlarged cavity



**Fig. 16** Resistance-ratio-change of the heater element versus input current. Thermal isolation effects of the cavity and the wiring-bridge were evaluated. (a) No cavity and no wiring-bridge; (b) No cavity under the heater, but having wiring-bridge at the both ends of the heater; and (c) Having both the thermal isolation cavity under the heater element, and the structure of wiring-bridge.



**Fig. 17** Experimental results of the fast response on the heater elements. Picture is got from the output wave in digital oscilloscope. When a 20- $\mu\text{s}$  of pulse voltage  $U_1$  is applied to the detection circuit, the voltage drop on the heater element reached its steady value of  $U_2$  in about 3- $\mu\text{s}$  of time.

#### E. Thermal response

Figure 17 shows the experimental result of the thermal response on the prototype. The detecting circuit was the same as in Fig. 8, except that the sensor sample was not in the oven but in the atmosphere. The experiment was carried out in 18 °C of room temperature. Increasing with the input voltage  $U_1$ , the voltage drop  $U_2$  in the heater element is increasing, but the voltage ratio  $U_2/U_1$  is decreasing due to the negative TCR of the heater element. From the experiment, it was found that the proposed sensor element shows very fast response to the temperature rise. As shown in Fig. 17, when a 0.4V/20- $\mu\text{s}$  of pulse voltage  $U_2$  was applied to the heater element, the steady maximum value of the voltage can be reached in about 3- $\mu\text{s}$  of time. According to the TCR, the temperature on the heater element was risen from the room temperature of 18 °C to the near 28 °C in 3- $\mu\text{s}$  of time. Such a high speed of response is a big advantage in the application of real time measurement of physical parameters like temperature or flow as well as distributed information including fingerprint patterns.

#### IV. SUMMARY

Based on the simulation results of our previous work “Structural design points in arrayed micro thermal sensors (I) ~ Silicon-based approach ~”, we proposed useful thermal sensor structures and developed the fabrication process technology and verified effectiveness of the proposed design points by experiments using the fabricated prototypes.

The following conclusions can be summarized:

- (1) By front-undercut bulk micromachining technology, one-dimensional array of as small as  $5 \times 17 \times 50$  ( $\mu\text{m}^3$ ) of air-bridge micro heater elements with an 80- $\mu\text{m}$  of pitch was realized.
- (2) Wiring-bridge structure and metal film wiring are an effective solution to avoid an open-circuit on the step-wall and at the same time can efficiently control the heat loss

through the wiring. At 0.3-mA input current, about 20°C higher of temperature rise was obtained by means of wiring-bridge structure;

(3) By the structure of wiring-bridge and the isolation cavity underneath the heater element, the thermal capacity of the heater element is greatly reduced that results in very high thermal response for the sensor. As fast as  $\mu$ s of thermal response was realized on the prototype. Application of a sensitive micro temperature sensors and micro flow sensors is promising by this structure.

(4)  $\text{SiO}_2$  layer can result in a big temperature gradient, and the insulation effect shows linear increase with its thickness. However, in order to get further of isolation results, it is not a good solution to increase  $\text{SiO}_2$  layer thickness over 2- $\mu\text{m}$  because of the time consuming and cost problem of the process.

(5) 100- $\mu\text{m}$  deep of cavity under the heater element cannot satisfy effective thermal isolation and mechanical strength when considering the application of fingerprint sensor.

There are following two possible approaches can be considered for the most serious application of fingerprint sensor: Silicon-based approach and polymer-based approach.

In silicon-based approach, in order to realize applicable sensitivity, the cavity needs to be enlarged further by etching out the substrate even to the whole area of sensing element including the area of wiring-contact or even under the wiring-support. By this solution, the applications of distribution measurement like temperature or flow become much advantageous, but for the application of fingerprint sensor, it is a desirable way to fill the etched cavity with thermal insulation materials to ensure enough strength for the fingertip pressure.

In our previous work, it was known that over 80 % of the input power was consumed at the substrate. Thermal conductivity of the substrate was the most sensitive parameter and the idea of thermal isolation from the heater element to the substrate is the most important key point in the structural design to realize a high resolution and sensitive micro thermal sensors.

In polymer-based approach, the combination of polymer substrate with platinum film sensing element will be a cost-effective and a promising solution to realize the proposed fingerprint capture.

For the limit to the number of page, the polymer-based approach will be reported in another paper “Structural design points in arrayed micro thermal sensors (III) ~ Polymer-based approach ~”.

Thermal Aspects in Microsystem Technology (Invited Paper), Budapest, 1998, 133-141.

- [5] P. M. Sarro, H. Yashiro, A. W. V. Herwaarden, S. Middelhoek, An integrated thermal infrared sensing array, Sensors and Actuators, 14 (1988) 191-201.
- [6] W. Schnelle, U. Dillner, S. poster, A linear thermopile infrared sensing array, VDI-Berichte, 982, (1992) 261-264.
- [7] R. Lenggenhager, H. Baltes, T. Elbel, Thermoelectric infrared sensors in CMOS technology, Sensors and Actuators, A37-38 (1993) 216-220.
- [8] A. D. Oliver, W. G. Baer, K. D. Wise, A bulk-micromachined 1024-element uncooled infrared imager, Transducers'95 Digest of Technical Papers, Vol. 2, Stockholm, 1995, 636-639.
- [9] C. M. Travers, A. Jahanzeb, D. P. Butler, Z. Celik-Butler, Fabrication of semiconducting  $\text{YBaCuO}$  surface-micromachined bolometer arrays, J. Microelectromech. Systems, 6 (1997) 271-276.
- [10] T. Kanno, M. Saga, S. Matsumoto, M. Uchida, N. Tsukamoto, A. Tanaka, S. Itoh, A. Nakazato, T. Endoh, S. Tohyama, Y. Yamamoto, S. Murashima, N. Fujimoto, N. Teranishi, Uncooled infrared focal plane array having 128'128 thermopile detector elements, Proc. SPIE, 2269 (1994) 450-459.
- [11] K. C. Liddiard, M. H. Unewisse, O. Reinhold, Design and fabrication of thin film monolithic uncooled infrared detector arrays, Proc. SPIE, 2225 (1994) 62-71.
- [12] A. Tanaka, S. Matsumoto, N. Tsukamoto, S. Itoh, T. Endoh, A. Nakazato, Y. Kumazawa, M. Hijikawah, H. Gotoh, T. tanaka, N. Teranishi, Silicon IC process compatible bolometerinfrared focal plane array, Transducers'95 Digest of Technical papers, Vol. 2, Stockholm, 1995, 632-635.
- [13] H. Jerominek, F. Picard, N. R. Swart, M. Renaud, M. Levesque, M. Lehoux, J. S. Castonguay, M. Pelletier, G. Bilodeau, D. Audet, T. D. Pope, P. Lambert, Micromachined, uncooled,  $\text{VO}_2$ -based IR bolometer arrays, Proc. SPIE, 2746 (1996) 60-71.
- [14] K. Sato, K. Asaumi, G. Kobayashi, Y. Iriye, “Development of an orientation-dependent anisotropic etching simulation system MICROCAD”, Electronics and Communications in Japan, Part 2, Vol. 83, No. 4, 2000, 13-22.
- [15] J. W. Gardner, “Microsensors, Principles and Applications”, John Wiley & Sons, Chichester, 1994.
- [16] Toyota Central R&D Labs., Inc., “Piezoelectric semiconductors and its applications”, 1970.
- [17] W. R. Runyan, “Silicon semiconductor technology”, McGraw-Hill, New York, 1965.
- [18] Helmut F. Wolf, “Silicon Semiconductor Data”, Pergamon Press, New York, 1969.
- [19] G. Bertolini, A. Coche, “Semiconductor Technology”, North-Holland, Amsterdam, 1968

## REFERENCES

- [1] I. H. Choi, K. D. Wise, A silicon-thermopile-based infrared sensing array for use in automated manufacturing, IEEE Trans. On Electron Devices, ED-33 (1986) 72-79.
- [2] R. A. Wood, Uncooled thermal imaging with monolithic silicon focal planes, Proc. SPIE, 2020 (1993) 322-329.
- [3] H. Jerominek, M. Renaud, N. R. Swart, F. Picard, T. D. Pope, M. Levesque, M. Lehoux, G. Bilodeau, M. Pelletier, D. Audet, P. Lambert, Micromachined  $\text{VO}_2$ -based uncooled IR bolometric detector arrays with integrated CMOS readout electronics, Proc. SPIE, 2882 (1996) 111-121.
- [4] U. Dillner, Thermal simulation and realization of micromachined thermal sensor arrays, Proceedings of 5th NEXUSPAN Workshop on